

Process Layout and Function Calls

CS 161 – Spring 2013

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Vallentin

January 23, 2013



Zero Day

Ryan Naraine and Daniel Kennedy

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Google pays \$14,000 for high-risk Chrome security holes

By Ryan Naraine | January 14, 2011, 9:52am PST

Summary

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The latest Google Chrome 8.0.552.237, available for all platforms, patches a total of 16 documented vulnerabilities, including one critical bug for which Google paid the first elite \$3133.7 award to researcher Sergey Glazunov.

"Critical bugs are harder to come by in Chrome, but Sergey has done it," says Google's Jerome Kersey. "Sergey also collects a \$1337 reward and several other rewards at the same time, so congratulations Sergey!" he added.

Topics

Google Inc., Team, Adobe PDF, CERT,



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Outline

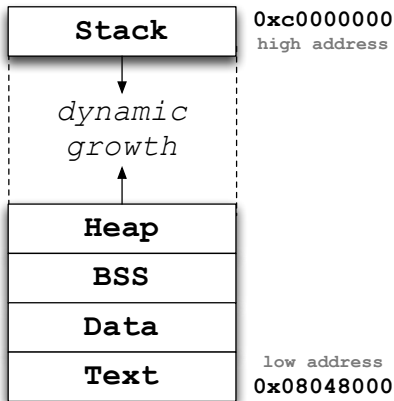
Process Layout

MIPS → IA-32

Function Calls

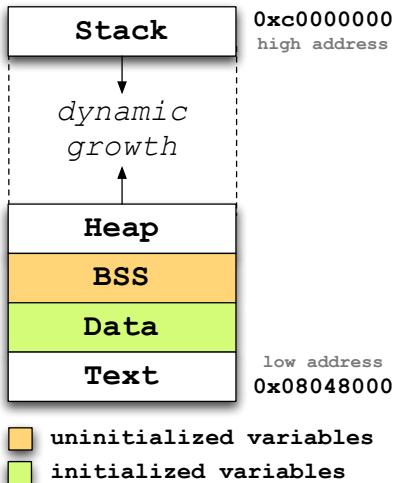
Process Layout in Memory

- ▶ **Stack**
 - ▶ grows towards *decreasing* addresses.
 - ▶ is initialized at *run-time*.
- ▶ **Heap**
 - ▶ grow towards *increasing* addresses.
 - ▶ is initialized at *run-time*.
- ▶ **BSS** section
 - ▶ size fixed at *compile-time*.
 - ▶ is initialized at *run-time*.
 - ▶ was grouped into **Data** in CS61C.
- ▶ **Data** section
 - ▶ is initialized at *compile-time*.
- ▶ **Text** section
 - ▶ holds the program instructions (read-only).



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Outline

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MIPS → IA-32: Differences

▶ RISC vs CISC

- ▶ IA-32 has many more instructions
- ▶ IA-32 instructions are variable length
- ▶ IA-32 instructions can have implicit arguments and side effects

▶ Limited Number of Registers

- ▶ MIPS has 18 general purpose registers (\$s0-\$s7, \$t0-\$t9)
- ▶ IA-32 has 6 (%eax, %edx, %ecx, %ebx, %esi, %edi)
 - ▶ This means lots of stack operations!

▶ Operand Directions

- ▶ MIPS: mov dst src
- ▶ IA-32: mov src dst

▶ Memory operations

- ▶ Very common to see push/pop/mov in IA-32
 - ▶ We'll see more of this later

▶ The list goes on!

MIPS → IA-32

Registers

Use	MIPS	IA32	Notes
Program Counter	PC	%eip	Can not be referenced directly
Stack Pointer	\$sp	%esp	
Frame Pointer	\$fp	%ebp	
Return Address	\$ra	-	RA kept on stack in IA-32
Return Value (32 bit)	\$v0	%eax	%eax not used solely for RV
Argument Registers	\$a0-\$a3	-	Passed on stack in IA-32
Zero	\$0	-	Use immediate value on IA-32

Register Terminology

SFP **saved frame pointer**: saved %ebp on the stack

OFF **old frame pointer**: old %ebp from the previous stack frame

RIP **return instruction pointer**: return address on the stack

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Function Calls

Function Calls

```
void foo(int a, int b, int c)
{
    int bar[2];
    char qux[3];
    bar[0] = 'A';
    qux[0] = 0x42;
}
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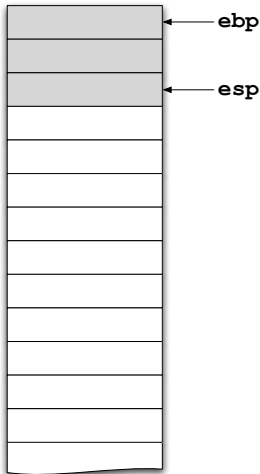
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int main(void)
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Function Calls in Assembler

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main:

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    pushl %ebp
    movl  %esp,%ebp
    subl  $4,%esp
    movl  $1,-4(%ebp)
    pushl $3
    pushl $2
    pushl $1
    call  foo
    addl  $12,%esp
    xorl  %eax,%eax
    leave
    ret
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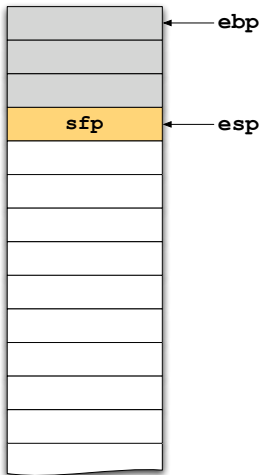


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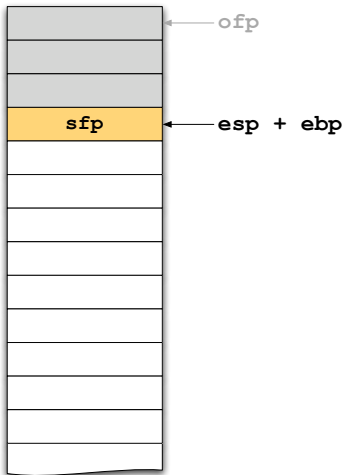


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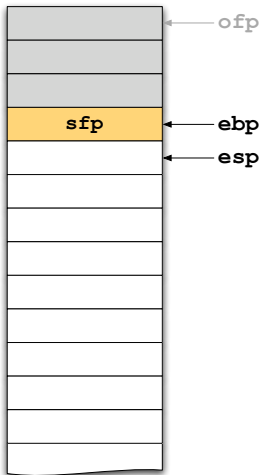
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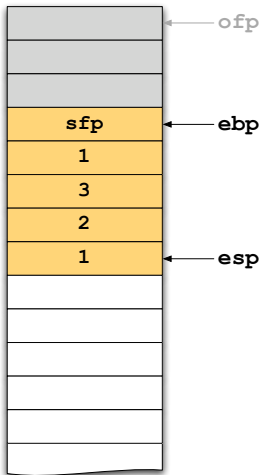
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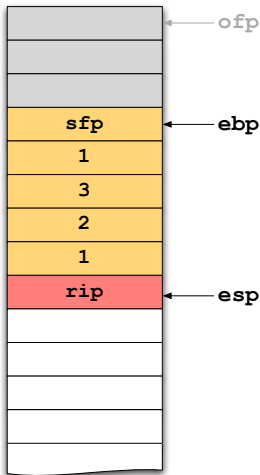
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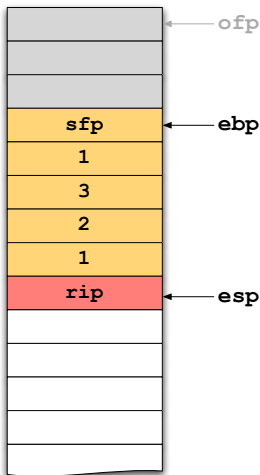


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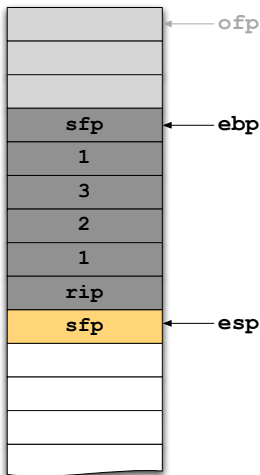


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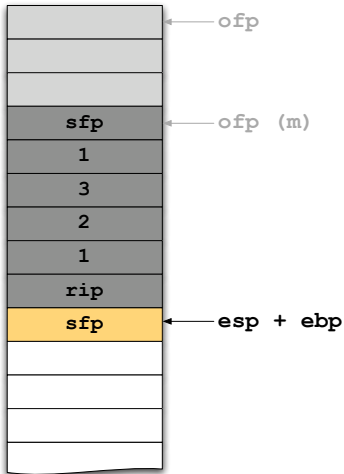


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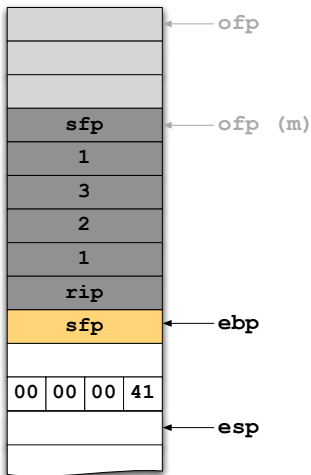


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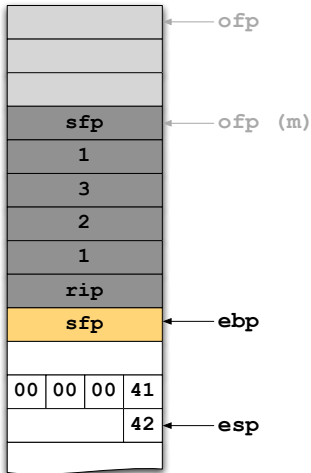


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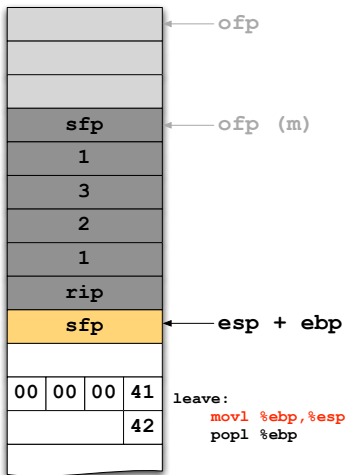


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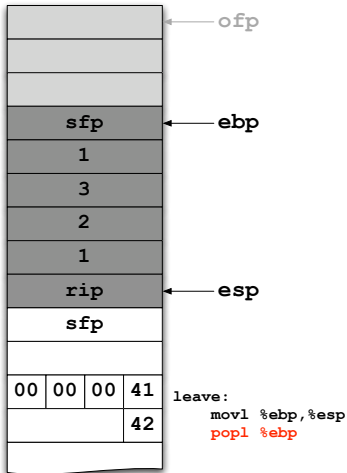


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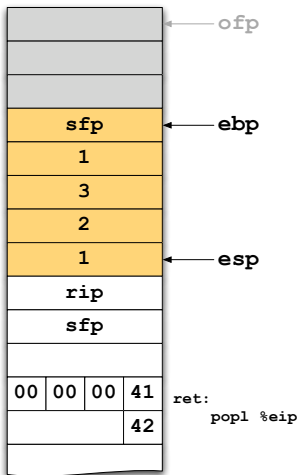


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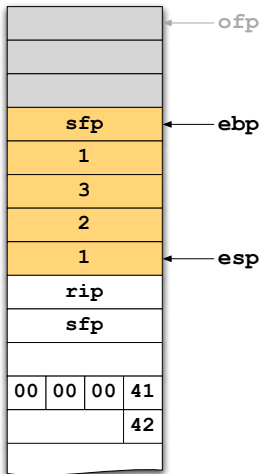
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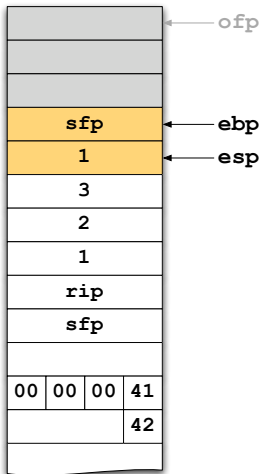
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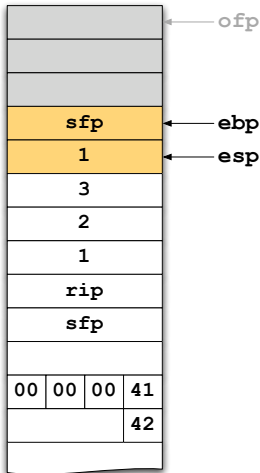
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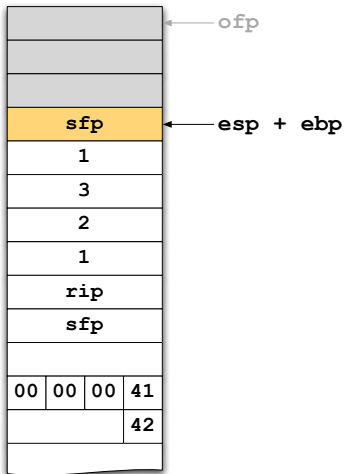
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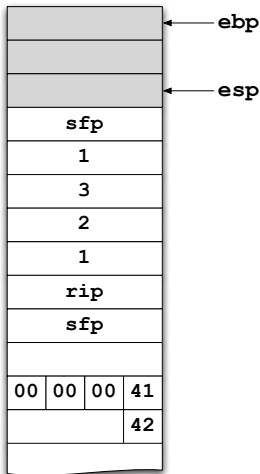
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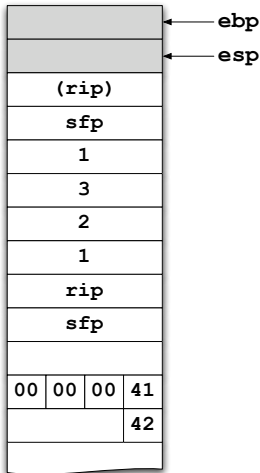
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IA-32 Reference

IA32 Instructions

<code>movl Src, Dest</code>	<i>Dest = Src</i>
<code>addl Src, Dest</code>	<i>Dest = Dest + Src</i>
<code>subl Src, Dest</code>	<i>Dest = Dest - Src</i>
<code>imull Src, Dest</code>	<i>Dest = Dest * Src</i>
<code>sall Src, Dest</code>	<i>Dest = Dest << Src</i>
<code>sarl Src, Dest</code>	<i>Dest = Dest >> Src</i>
<code>shrl Src, Dest</code>	<i>Dest = Dest >> Src</i>
<code>xorl Src, Dest</code>	<i>Dest = Dest ^ Src</i>
<code>andl Src, Dest</code>	<i>Dest = Dest & Src</i>
<code>orl Src, Dest</code>	<i>Dest = Dest Src</i>
<code>incl Dest</code>	<i>Dest = Dest + 1</i>
<code>decl Dest</code>	<i>Dest = Dest - 1</i>
<code>negl Dest</code>	<i>Dest = - Dest</i>
<code>notl Dest</code>	<i>Dest = ~ Dest</i>
<code>leal Src, Dest</code>	<i>Dest = address of Src</i>
<code>cmpl Src2, Src1</code>	<i>Sets CCs Src1 - Src2</i>
<code>testl Src2, Src1</code>	<i>Sets CCs Src1 & Src2</i>
<code>jmp label</code>	<i>jump</i>
<code>je label</code>	<i>jump equal</i>
<code>jne label</code>	<i>jump not equal</i>
<code>js label</code>	<i>jump negative</i>
<code>jns label</code>	<i>jump non-negative</i>
<code>jl label</code>	<i>jump greater (signed)</i>
<code>jge label</code>	<i>jump greater or equal (signed)</i>
<code>jl label</code>	<i>jump less (signed)</i>
<code>jle label</code>	<i>jump less or equal (signed)</i>
<code>ja label</code>	<i>jump above (unsigned)</i>
<code>jb label</code>	<i>jump below (unsigned)</i>

Addressing Modes

Immediate	<i>Sval</i>	<i>Val</i>
Normal	(R)	Mem[Reg[R]]
	•Register R specifies memory address	
	<code>movl (%ecx), %eax</code>	
Displacement	D(R)	Mem[Reg[R]+D]
	•Register R specifies start of memory region	
	•Constant displacement D specifies offset	
	<code>movl 8(%ebp), %edx</code>	
Indexed	D(Rb, Ri, S)	Mem[Reg[Rb]+S*Reg[Ri]+ D]
	•D: Constant "displacement" 1, 2, or 4 bytes	
	•Rb: Base register: Any of 8 integer registers	
	•Ri: Index register:	
	•S: Scale: 1, 2, 4, or 8	

Condition Codes

CF	Carry Flag
ZF	Zero Flag
SF	Sign Flag
OF	Overflow Flag

`%eax``%edx``%ecx``%ebx``%esi``%edi``%esp``%ebp`

Additional references will be posted on Piazza